ECR#: P28
Tracker #: 32
Status: Ratified
Title: Clarification to ECR# P21 (3.3Vaux signal definition for compliance with PCI 2.2 (PM 1.1)
Release Date: March 1999
Impact, High: Change to electrical portion of specification
Spec Version: NLX Motherboard Specification V1.2
NLX Electrical Design Suggestions V1.21

Summary:

This ECR amends ECR# P21 that was published on the NLX Web site in October 1998. ECR# P21 defined a pin for 3.3V Standby (3.3Vaux) on the NLX riser. The change was necessary, because to comply with the *Peripheral Component Interconnect Specification* (PCI V2.2 [PM 1.1]), a system must be able to provide standby power to pin 14A of the PCI connectors on the riser.

This new ECR# 28 does not include any additional technical change from that described in ECR# P21. Instead, this ECR provides the necessary pointers to text locations that should have been modified via ECR# P21.

Although this ECR assumes that you previously applied to your specification the pin changes to Table 4.10 described in ECR# P21, for your convenience the change to Table 4.10 is repeated here.

Two different documents are affected (see "Spec Version," above.)

CHANGE the *NLX Motherboard Specification,* V1.2, as Shown:

In Table 4.3, list an additional power signal.

ORIGINAL plus ECR 25:

Table 4.3: Power Pins/Signals, Total of 67

Signal Group	Number of Signals
5VDC	13
3.3VDC	13
SENSE3.3	1
-5V	1
-12V	1
+12V	3
Ground	31
Power Supply On/Off	1
Soft On/Off	1
Powergood	1
5VSB	1

CHANGE per this ECR:

Table 4.3: Power Pins/Signals, Total of 68

Signal Group	Number of Signals
5VDC	13
3.3VDC	13
SENSE3.3	1
-5V	1
-12V	1
+12V	3
Ground	31
Power Supply On/Off	1
Soft On/Off	1
Powergood	1
5VSB	1
3.3Vaux	1

In Table 4.7, make sure the number of Reserved pins equals four (applying changes from ECRs 14, 21, and 25).

ORIGINAL plus CHANGES from ECRs 14, 21, and 25:

Table 4.7: Miscellaneous and Front Panel Signals, Total of 30

Signal Group	Number of Signals
Reserved	4
Infra-Red	5
Power LED	1
Front Panel Sleep	1
Modem Wake Up	1
LAN Wake Up	1
LAN Activity	1
Front Panel Reset	1
USB	6
Fan Control	4
Tamper Detection	1
VBAT	1
Message Waiting	1
Serial bus	2

*In Table 4.10, make sure that the change to pin A135 (ECR# 21) has been applied to the table and that the new footnote from ECR# 21 has been added below the table (footnote text = * Pin A135 is rated at 2A).*

ORIGINAL plus ECR# 21:

Table 4.10: IDE, Floppy, and Front Panel Section, Riser Interconnect Pin-out

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
…					…				
A135	RESERVED	RES	N/A	N/A	…				

CHANGE:

Table 4.10: IDE, Floppy, and Front Panel Section, Riser Interconnect Pin-out

Pin	Signal Name	Type	I/O	Termination	Pin	Signal Name	Type	I/O	Termination
…					…				
A135*	3.3Vaux	PWR	O	N/A	…				

* Pin A135 is rated at 2A.

In Table 4.11, remove the reference to pin A135 as reserved.

ORIGINAL plus CHANGES from ECRs 14, 21, and 25:

Table 4.11: IDE, Floppy, and Front Panel Signal Descriptions

Signal	Pin	I/O	Description	Signal Type
Reserved RESERVED	 A116 A140 B166 A167	 N/A N/A N/A N/A	These pins should not be used for any purpose. They are reserved to allow compatibility with future implementations of the interface; compatibility problems can result if these signals are misused.	N/A

In Table A.3, add an entry for the +3.3Vaux voltage tolerance.

ORIGINAL:

Table A.3, Recommended Voltage Tolerances for Motherboard at Riser Connection

Voltage	Tolerance
+5V	±5 %
-5V	±5 %
+12V	±5 %
-12V	±5 %
+3.3V	±4 %
Standby +5V	±5 %

CHANGE:

Table A.3, Recommended Voltage Tolerances for Motherboard at Riser Connection

Voltage	Tolerance
+5V	±5 %
-5V	±5 %
+12V	±5 %
-12V	±5 %
+3.3V	±4 %
+3.3V Auxiliary	±4%
Standby +5V	±5 %

NLX Electrical Design Suggestions, V1.21, Change the Current Design Document as Shown:

Insert a NEW section after Section 2.5.6.

2.5.7 3.3Vaux

3.3Vaux is generated on the motherboard and delivered to the riser. This power signal should be used to power PCI devices that require auxiliary 3V and should be routed to the 3.3Vaux pin on PCI connectors. Note that NLX pin A135 is rated at 2A.

Modify Section 3.1.5 to include 3.3Vaux as one of the "other power sources," listed in the second bulleted item below the section header.

ORIGINAL:

- +12V, -12V, -5V, 5VSB—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.

CHANGE, per this ECR:

- +12V, -12V, -5V, 5VSB, 3.3Vaux—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.

Modify Section 4.5 to add 3.3Vaux to the second bulleted item below Figure 15.

ORIGINAL:

— +12V, -12V, -5V, 5VSB—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.

CHANGE, per this ECR:

— +12V, -12V, -5V, 5VSB, 3.3Vaux—These other power sources are typically routed as thick traces. Bulk and decoupling capacitors should be added to support the power requirements of the system.

Modify the Power Signals section under Section 4.7, NLX Motherboard Checklist, to add 3.3Vaux to the second bulleted item below the Power Signals heading.

ORIGINAL:

— 5VDC/3.3VDC/+12V/-12V/IEEE-1394/Powergood/5VSB—Ensure signals are routed as a plane or thick traces.

CHANGE, per this ECR:

— 5VDC/3.3VDC/+12V/-12V/IEEE-1394/Powergood/5VSB/3.3Vaux—Ensure signals are routed as a plane or thick traces.